Roshan Yan

Toronto, Ontario, Canada | roshan.yan@mail.utoronto.ca | +1 647 916 3425 | roshanyan.ca | linkedin.com/in/roshan-yan

Education

University of Toronto – BASc in Electrical Engineering + PEY Co-op Sep 2024 – Expected Apr 2029

- CGPA: 3.54/4.00

Experience

Summer Research Intern, Power Management & SMPS Laboratory – Toronto, ON Apr 2026 – Present

- Designed and prototyped a 48 V-to-1 V multiphase quasi-resonant buck converter using resonant flying-capacitor operation for soft switching at high conversion ratios, leveraging GaN devices.
- Developed converter operating modes and control timing in PLECS and experimentally characterized prototype switching behavior and efficiency.

Electrical Power Systems Lead, University of Toronto Aerospace Team – Toronto, ON Sep 2024 – Present

- Lead a 5-member team developing the EPS for a 3U CubeSat.
- Led development of a 6-layer EPS PCB for up to 10 W solar input, integrating buck MPPT, a 2S2P 21700 battery pack, and regulated 5 V/3.3 V rails.
- Implemented inter-stage voltage/current monitoring and handled component selection, Altium PCB design, assembly, and testing.

Summer Research Intern, In Situ and Correlative Microscopy Group – Toronto, ON May 2025 – Aug 2025

- Modeled pressure-driven deflection and failure of silicon nitride membranes using ANSYS Mechanical.
- Investigated thin-film residual stress and developed FEA/CFD models to evaluate microscale device design trade-offs.

Technical Projects

Wideband Active Oscilloscope Probe

- Designed and hand-fabricated a DC-coupled active probe with approximately 3 pF input capacitance and controlled-impedance PCB routing.
- Characterized response using a VNA, measuring approximately 650 MHz -3 dB bandwidth; diagnosed probe-induced resonance and developed damping networks.

TinyTapeout 6502-Style CPU & PLL

- Collaborated on a compact 6502-inspired CPU, progressing from concept to TT26C tapeout in approximately 1.5 weeks using tiles obtained through FOSSi.
- Designed and simulated a ring-oscillator PLL in xschem and ngspice to generate a high-speed internal CPU clock independent of the TinyTapeout multiplexed I/O clock.
- Completed schematic design and physical layout of the PLL through GDS generation; the block was excluded from the submitted design due to shuttle area constraints.

FPGA CORDIC Spectrum Analyzer

- Implemented vectoring and rotation CORDIC blocks in Verilog for quadrature down-conversion and phase/magnitude extraction.
- Built a zero-IF digital receiver chain with complex mixing, low-pass filtering, decimation, and envelope detection.
- Developed HDL testbenches using known-tone stimuli to verify mixer, CORDIC, phase, and magnitude accuracy.

C-Band Negative-Resistance VCO

- Designed a discrete C-band negative-resistance VCO in Cadence AWR for an ISM-band radar application using a lumped-element series resonant network.
- Performed RF simulation and tuning-network optimization to improve oscillation margin, tuning range, and frequency-control linearity; prototype PCB in fabrication.

Hackathons & Leadership

U of T IEEE ASIC Hackathon – Honourable Mention Feb 2026

- Collaborated in a team of three to develop a hardware ray-tracing accelerator targeting TinyTapeout.
- Designed direct FPGA-to-VGA demonstration hardware and conducted RTL functional verification and timing analysis.

Skills

- **PCB & Circuit Design:** Altium Designer, KiCad, LTspice, PSpice, PLECS, TINA-TI
- **RF & ASIC:** Keysight ADS, Cadence AWR, HFSS, Maxwell, Verilog, xschem, ngspice, timing analysis
- **Programming:** Python, MATLAB, PyVISA
- **Lab & Fabrication:** VNA, spectrum analyzer, oscilloscope, soldering/rework, machining, 3D printing, ANSYS Mechanical

Certifications

Canadian Advanced Amateur Radio Qualification | Machining Fundamentals, George Brown College, 2025